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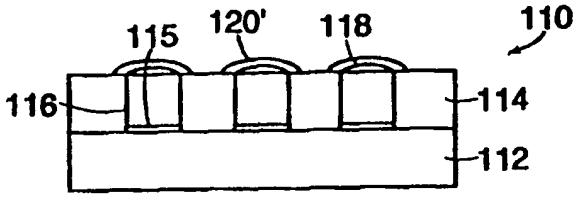
(54) Title: FLIP CHIP WITH INTEGRATED FLUX, MASK AND UNDERFILL

(57) Abstract

A flip chip having solder bumps (118), an integrated underfill (114), and a separate flux coating (120), as well as methods for making such a device, is described. The device is characterized in that the underfill material (114) is provided on the chip surface prior to the application of solder bumps, and then optionally treated to form apertures (116) therein which act as a mask for solder bump application. The resulting device is well suited for a simple one-step application to a printed circuit board, thereby simplifying flip chip manufacturing processes which heretofore have required a separate underfilling step.



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FLIP CHIP WITH INTEGRATED FLUX, MASK AND UNDERFILL

Field of the Invention

The present invention relates to a novel flip chip design. More particularly, the present invention relates to a flip chip which incorporates solder bumps, flux and an underfill material, wherein the underfill material acts as a mask during application of the solder bumps.

Background of the Invention

In the electronics industry, electrical components such as resisters, capacitors, inductors, transistors, integrated circuits, chip carriers and the like are typically mounted on circuit boards in one of two ways. In the first way, the components are mounted on one side of the board and leads from the components extend through holes in the board and are soldered on the opposite side of the board. In the second way, the components are soldered to the same side of the board upon which they are mounted. These latter devices are said to be "surface-mounted."

Surface mounting of electronic components is a desirable technique in that it may be used to fabricate very small circuit structures and in that it lends itself well to process automation. One family of surface-mounted devices, referred to as "flip chips", comprises integrated circuit devices having numerous connecting leads attached to pads mounted on the underside of the device. In connection with the use of flip chips, either the circuit board or the chip is provided with small bumps or balls of solder (hereafter "bumps" or "solder bumps") positioned in locations which correspond to the pads on the underside of each chip and on the surface of the circuit board. The chip is mounted by (a) placing it in contact with the board such that the solder bumps become sandwiched between the pads on the board and the corresponding pads on the chip; (b) heating the assembly to a point at which the solder is caused to reflow (i.e., melt); and (c) cooling the assembly. Upon cooling, the solder hardens, thereby mounting the flip chip to the board's surface. Tolerances in devices using flip chip technology are critical, as the spacing between individual devices as well as the spacing between the chip and the board is typically very small. For example, spacing of such chips from the surface of the board is typically in the range of 0.5-3.0 mil and is expected to approach micron spacing in the near future.

One problem associated with flip chip technology is that the chips, the solder and the material forming the circuit board often have significantly different coefficients of thermal expansion. As a result, differing expansions as the assembly heats during use can cause severe

stresses, i.e., thermomechanical fatigue, at the chip connections and can lead to failures which degrade device performance or incapacitate the device entirely.

In order to minimize thermomechanical fatigue resulting from different thermal expansions, thermoset epoxies have been used. Specifically, these epoxies are used as an underfill material which surrounds the periphery of the flip chip and occupies the space beneath the chip between the underside of the chip and the board which is not occupied by solder. Such epoxy systems provide a level of protection by forming a physical barrier which resists or reduces different expansions among the components of the device.

Improved underfill materials have been developed in which the epoxy thermoset material is provided with a silica powder filler. By varying the amount of filler material, it is possible to cause the coefficient of thermal expansion of the filled epoxy thermoset to match that of the solder. In so doing, relative movement between the underside of the flip chip and the solder connections, resulting from their differing coefficients of thermal expansion, is minimized. Such filled epoxy thermosets therefore reduce the likelihood of device failure resulting from thermomechanical fatigue during operation of the device.

While underfill has solved the thermal mismatch problem for flip chips on printed circuit boards, it has created significant difficulties in the manufacturing process. For example, the underfill must be applied off-line using special equipment. Typically, the underfill is applied to up to three edges of the assembled flip chip and allowed to flow all the way under the chip. Once the material has flowed to opposite edges and all air has been displaced from under the chip, additional underfill is dispensed to the outer edges so as to form a fillet making all four edges symmetrical. This improves reliability and appearance. Next, the assembly is baked in an oven to harden the underfill. This process, which may take up to several hours, is necessary to harden and fully cure the underfill. Thus, although the underfill solves the thermal mismatch problem and provides a commercially viable solution, a simpler manufacturing method would be desirable.

Recently, attempts have been made to improve and streamline the underfill process. One method that has shown some commercial potential involves dispensing underfill before assembling the flip chip to the board. This method requires that the underfill allow solder joint formation to occur. Soldering of flip chips to printed circuit boards is generally accomplished by applying flux to the solder bumps on the flip chip or to the circuit pads on the printed circuit board. Thus, it has been suggested to use an underfill that is dispensed first, prior to making solder connections. In order to facilitate solder bonding, however, the underfill must contain flux

or have inherent properties that facilitate solder joint formation. Flux is used since the pads on printed circuit boards often oxidize, and since solder bumps on flip chips are always oxidized. Thus, the flux is designed to remove the oxide layers facilitating solder joint formation.

Certain underfills commonly called "dispense first underfills" have been designed with self-contained flux chemistry. Unfortunately, the properties required for a good flux and those required for a good underfill are not totally compatible. As such, a compromise of properties results. The best flux/underfill materials typically require more than an hour to harden. Additionally, flux-containing underfills still require the use of special equipment including robot dispensing machines. Also, since solder assembly and underfill application are combined into a single step, the flip chip cannot be tested until the assembly is complete. Thus, if the chip does not operate satisfactorily, it cannot be removed because the underfill will have hardened, thereby preventing reworking.

Finally, certain problems have been found to arise when applying flux/underfill materials to bumped surfaces of flip chips. The problems result because the rough surface geometry of the bumped surface is not readily amenable to the application of fluids, particularly those having high viscosity. Thus, Providing the flux/underfill directly onto a bumped surface raises at least the possibility of discontinuities and air bubbles forming during the flux/underfill application process. Furthermore, by eliminating bumping prior to application of the flux/underfill layer, it may be possible to eliminate process steps, thereby streamlining the manufacturing process while providing chip makers with greater design and manufacturing flexibility.

In view of the above, a need still exists for a more efficient process that reduces the need for expensive equipment and that is compatible with existing electronic device assembly lines. A need for a reworkable underfill also exists. A further need exists for a flux/underfill material that can optionally act as a mask during the bumping steps as well.

Summary of the Invention

The present invention relates to an integrated circuit assembly comprising a semiconductor wafer which includes solder bumps, flux, and an underfill material. In a broad sense, the invention relates to an integrated circuit assembly which includes a substrate having a plurality of solderable contact sites on one surface and a plurality of solder bumps positioned on that surface such that each of the solderable contact sites has one solder bump associated with and affixed to each solderable contact site. Each site further includes a flux material which covers at least a portion of each solder bump and an underfill material which occupies the space

defined between each of the solder bumps. The underfill material is of a depth such that at least a flux covered portion of each solder bump extends above the underfill. In the present case, the underfill material can be applied to the wafer prior to or after applying the solder bumps. If applied first, the underfill can then be processed to convert it into a mask to assist in placement of the bumps onto the wafer surface.

The present invention also relates to a method for making an integrated circuit assembly which includes the steps of providing a substrate having a plurality of solderable contact sites on a surface thereof, positioning a plurality of solder bumps on the substrate such that each of the solderable contact sites has one solder bump associated with it, and affixing each solder bump to its associated contact site. Once the solder bumps are mounted, a flux material is applied to the solder bumps in a manner such that at least a portion of each solder bump is provided with flux. Finally, an underfill material is applied to the surface of the substrate. The underfill occupies the space defined between each of the solder bumps and has a depth such that at least a flux covered portion of each solder bump extends through the underfill.

The present invention also relates to a method for making an integrated circuit assembly which includes the steps of providing a substrate having a plurality of solderable contact sites on a surface thereof. An underfill material is applied to the surface of the substrate. Subsequently, the underfill is treated to form gaps therein at each of the solderable contact sites. The resulting underfill mask simplifies application of the solder bumps to the wafer in a manner such that each of the solderable contact sites has one solder bump associated with it. Each solder bump is then mounted to its associated contact site. Once the solder bumps are mounted, a flux material is applied to the solder bumps in a manner such that at least a portion of each solder bump is provided with flux. The resulting wafer is characterized in that the underfill occupies the space defined between each of the solder bumps and has a depth such that at least a flux covered portion of each solder bump extends through the underfill.

Lastly, the invention relates to a process for affixing a flip chip to a circuit board. The method involves providing a printed circuit board having a plurality of solderable contact sites on a surface, providing an integrated circuit chip of the type described above (i.e., a chip having solder bumps, flux and an underfill material present on its surface), and positioning the integrated circuit chip relative to the printed circuit board such that each solder bump is in contact with a solderable contact site on the printed circuit board. Once positioned, the integrated circuit chip assembly is heated to a temperature sufficiently high to melt the solder and the underfill material.

Subsequently, the assembly is allowed to cool to a temperature which allows the solder and underfill material to solidify.

Brief Description of the Drawings

FIG. 1 is a schematic elevation of a wafer having solder bumps thereon.

FIGS. 2A and 2B are schematic depictions of an apparatus for providing a flux coating on solder bumps.

FIG. 3 is a schematic elevation of a flip chip having solder bumps, each such bump having a flux coating thereon.

FIG. 4 is a schematic elevation of the device of FIG. 3 having an underfill material applied between the solder bumps.

FIG. 5 is a schematic elevational view of an alternative embodiment of FIG. 4 in which the flux coating entirely surrounds each solder bump.

FIG. 6 is a schematic depiction of one embodiment of the invention in which a wafer has an underfill material formed thereon prior to application of solder bumps.

FIG. 7 is a schematic depiction of the device in FIG. 6 in which the underfill material has been treated to form apertures therein, the apertures allowing the underfill to act as a mask during solder bump application.

FIG. 8 is a schematic depiction of the device of FIG. 7 following application of solder bumps.

FIG. 9 is a schematic depiction of the device of FIG. 8 showing application of a flux layer over the solder bumps.

FIG. 10 is a schematic depiction of an alternate embodiment of the device of FIG. 9 showing application of a flux layer over the solder bumps only.

Detailed Description of the Invention

The present invention provides a unique method of applying fluxes and underfills during the flip chip mounting process. Specifically, the present invention relates to the application of underfill and flux at the wafer level before the wafer is divided into individual integrated circuits. Thus, in the present invention the underfill and flux are pre-applied and converted into a solid state. This process differs from other types of underfill application processes in which the underfill is present in the liquid state and then applied to the device at the point of chip assembly to the printed circuit board. Additionally, the underfill and the flux are separated, rather than

being mixed as a combined flux/underfill composition. As noted previously, liquid systems combine the flux and underfill systems into a single composition and, thus, provide neither flux nor underfill having ideal properties.

The present invention recognizes that flux is required only at the areas of the solder bumps, and not in the spaces in between those connecting elements. Thus, the present invention separates the flux from the underfill in the regions between the solder bumps. Furthermore, by maintaining the flux and underfill as separate entities, additives tailored to each individual component may be added to provide both the flux and the underfill with desired properties. For example, the underfill can be a thermoplastic that de-bonds at elevated temperatures, or the flux layer can be designed to de-bond. As an alternative, the flux can convert to a strongly-bonded polymer after its mission as a flux has been accomplished, and the underfill can have the de-bonding properties. As such, a system in which the flux and underfill are maintained as separate entities is extremely versatile.

Likewise, an alternative embodiment employs the use of an underfill only. In such a case, there would be a requirement that flux be added separately to the board or to the flip chip using any of the wide variety of processes that are currently in commercial use. Although an additional fluxing step would be required, the use of an underfill-only embodiment would still eliminate the necessity for the underfill process after the chip is mounted, while allowing the use of standard electronic component assembly equipment.

In one embodiment, the invention comprises the application of a layer of hardenable underfill to a bumped wafer followed by drying or hardening. The underfill material is preferably a thermoplastic or a thermoset having a very low crosslink density. In either case, the underfill material is filled with a low expansion inorganic particulate material such as silica. The resulting underfill should preferably have a coefficient of thermal expansion (CTE) that approximates that of the solder joint or other joining material. In the case of eutectic solder joints, the CTE should range from approximately twenty to thirty parts per million per °C. It is preferred that the resin system is soluble in a safe solvent system to allow the resin to be coated as a liquid in a viscosity range suitable for wafer-coating methods. Although a dry polymer film or powder could be coated onto the wafer by melting, a liquid is preferred because of the availability of wafer dispensing and coating equipment adapted to liquid handling processes. Additionally, this embodiment includes a layer of flux that is designed to be compatible with flip-chip assembly and underfills.

One such flux system includes epoxy resins and an organic carboxylic acid, an anhydride or a combination thereof, and is commercially available from Alpha Metals under the trade name ChipFlux 2020. This material is a carboxyacid system. (Anhydrides are used in related products, although the acid derivatives provide stronger flux activity and more consistency). Although this material is a paste made with liquid epoxy resins, the system can be readily modified for use in the present invention. For example, solid epoxy resins having slightly higher molecular weight than liquid epoxies can be substituted and used with carboxylic acid as the flux. Even with solid epoxy resins and carboxylic acid (which is a solid at room temperature), the system can easily be dissolved in polar solvents and can then be coated in a liquid state and dried to a solid film. Although the preferred flux application methods are spin coating, spraying, or stenciling, the wafer can also be coated using a dipping process in which the bump side of the wafer is pressed against a thin layer of flux on a dispensing drum consisting of a rotating platen disk and a doctor blade (described below) to control the liquid thickness.

Flip chips having integrated underfill and flux can be mounted on a printed circuit board as follows. An individual flip chip, with integrated underfill and flux, is placed in contact with the circuit board in a manner such that the solder bumps are aligned with conductive pads printed on the board. The assembly is then passed to a multi-zone re-flow soldering oven. The application of heat causes the flux to melt and activate. For applications using the solid ChipFlux 2020 described above and used in tests, the material is heated to about 80° C, however, the useful range is about 40° C to about 100° C. The activated flux removes oxide on the solder bumps as well as on the circuit board. As heating is continued to higher temperatures (typically by moving the assembly into a higher temperature zone of the oven), the solder bumps are caused to melt and form a metallurgical joint between the flip chip and the printed circuit board. At that elevated temperature, the flux becomes deactivated. For example, in the case of a carboxylic acid/epoxy flux system, the elevated temperature causes the acid to chemically combine with the epoxy and become neutralized so that there will be no tendency toward corrosion. Such fluxes are called "no clean" fluxes. These fluxes are typically heated to about 190° C to about 220° C, however, the lower end of the temperature range is preferred since the flux does most of its work at solder reflow temperatures. The flux deactivation process also tends to harden the flux and create a strong bond to the printed circuit board. Such a bond is very desirable, and results because the typical printed circuit board is made with epoxy, thereby enhancing the ability of the similar epoxy-based flux to bond to the board.

Since the flux and underfill are contained in separate layers in the devices of the present invention, it is not essential, although it is preferred, that the underfill layer melt. The underfill must soften and preferably melt so that it will wet out and bond to the circuit substrate. Since the maximum soldering temperature for common eutectic solder is about 220-225° C, the underfill will have softened and/or melted upon reaching this temperature. However, in the case where a higher melting underfill is needed, bonding can take place at the softening point if downward force is applied. It is preferred that only about half of the original bump height be covered with underfill since it is expected that the bump would typically collapse to about half of its original height as the solder wets the conductive pad on the printed circuit board and forms the joint.

After the solder has melted, the assembly is allowed to cool, thereby allowing the solder to harden and to form a solid metallurgical joint between the flip chip and the board. The resulting assembly is protected from thermomechanical strain by the underfill and flux layers. In one preferred embodiment, the flux may assume underfill properties as the result of polymerization.

The flux can be made into an underfill-like material by adding a sufficient low-expansion filler such as silica. It has been recognized that the flux polymerizes during the solder reflux process to a thermoplastic state. This means that the underfill and the flux can be reworked by heating the chip above solder reflow (i.e., about 200° C). This also means that any flux residue can be removed by a polar solvent if necessary. That result is optional, however, because most of the firm solder joint would be encased in the underfill composition which serves to provide optimum protective properties to the joint.

Alternatively, a standard flip chip bonder that can apply heat and pressure can be employed instead of the reflow oven. In that embodiment, the flip chip coated with the flux and underfill is placed into contact with the conductive pads on the circuit board and heat from the bonder head will activate the flux, form joints by reflowing the solder bumps, and cause the underfill and flux system to bond tightly to the board. The use of a standard flip chip bonder would allow a flip chip to be assembled to a board that already contained mounted components. This method could also be used to assemble a chip at a site that is being reworked.

Reworking is desirable in situations in which a chip mounting step has failed to properly position the chip on the board. Specifically, the assembly of fine pitch, high-density components can result in misalignments and failed connections. Furthermore, since it is difficult to fully test an unpackaged device such as a flip chip, it becomes desirable to be able to remove the chip if final testing indicates that the chip is not operating optimally, either through a fault with the chip

or as a result of improper mounting. Thermoset underfills do not allow the assembly to be reworked since thermosets cannot be melted once they have crosslinked.

The present invention eliminates the problems associated with thermoset underfills by incorporating a thermoplastic resin as the main component of the underfill. Thus, the chip can be removed by raising the chip temperature to above the melting point of the solder (approximately 183° C for tin/lead solder) and above the de-bonding temperature of the underfill resin. Typically, the rework temperature must be above the solder reflow temperature, but less than about 220° C depending on the circuit substrate. An average rework temperature would be about 200° C. The temperature can be higher if localized heat is used; for example, in an alternate embodiment, a chip bonder could be used to remove chips from a substrate post-bonding. In still another embodiment, the underfill may also include a B-staged thermoset that will de-polymerize at an elevated temperature.

Suitable thermoplastic resins include phenoxy, acrylic, methacrylic, polycarbonate, polyamides, polybutene, polyesters and some polyolefins. It is noted that the underfill does not need to be melted, rather, it is only necessary for the underfill to soften for de-bonding. Desirable polymers for use as thermoplastic underfill materials include thermoplastic die attach adhesives available from Alpha Metals under the trade name Staystik. Such materials can be de-bonded cleanly at elevated temperatures. Thus, when such materials are used, the thermoplastic film can be pealed away from both the chip and the circuit at elevated temperatures, leaving no residue.

Alternatively, the underfill can be made from a resin that is known to debond when a specific solvent is applied. One such resin system is a temporary attach adhesive available from Alpha Metals under the trade name Staystik 393. Underfills made with Staystik can be modified to contain a low expansion inorganic filler, preferably, a spherically-shaped silica of about 5 to about 15 microns in diameter. In order to achieve the desired coefficient of thermal expansion (CTE) close to that of tin/lead solder (22.5ppm/deg.° C), the underfill should comprise about 60 - 70% by weight silica and about 20 - 30% resin. Note that one advantage of using Staystik 393 is that it does not dissolve, but does debond in the presence of alcohol, thereby providing a system by which any residue can be easily removed.

An underfill made with resins of the type described above would allow the underfill to debond by adding alcohol around the chip site. That notwithstanding, however, the solder joints would still have to be heated to solder reflow temperatures to allow the chip to be removed.

Although either one of the flux or the underfill may be applied to the bumped chip first, it is preferred that the flux be applied prior to application of the underfill. This is because the surface energy properties of the interface between the bumps and the underfill can cause the underfill to creep up the side of the bump, thereby covering it entirely. This effect is undesirable because the underfill becomes positioned between the solder bump and the pad onto which the solder is intended to contact, thereby causing the underfill to act as a contaminant. To address this situation, flux is applied to the bumps first. In one preferred method, a dip-transfer process using a reservoir of flux paste can be used. This process is as described below.

FIG. 1 depicts a flip chip assembly 10 which comprises a wafer 12 having solder bumps 14 on its surface. Flux may be provided on the bumps 14 by means of the apparatus and process depicted in FIGS. 2A and 2B. Specifically, FIG. 2A is a top view of a flux application apparatus, and FIG. 2B is a side elevational view of that apparatus. In FIGS. 2A and 2B, the flux application apparatus 20 comprises a rotating platen 22 which communicates via a spindle 24 with a drive motor 26. A doctor blade 28 which may be adjusted to provide a gap of a predetermined distance above the platen is mounted on one side. A flux paste 30 is provided on the surface of the platen 22 upstream of the doctor blade. When the platen is rotated, the flux paste 30 is forced into the gap between the doctor blade 28 and the platen surface 22, thereby causing the flux paste downstream of the doctor blade to be at a predetermined and desired thickness. In one embodiment, it is preferred that the thickness of the flux paste 30 downstream of the doctor blade 28 is less than that of the height of each bump 14 above the wafer 12. The wafer is dipped into the reservoir of flux paste as can be seen in FIGS. 2A and 2B. Since the depth of the flux paste 30 is less than the height of the solder bumps 14, only a portion of the bumps will become coated with the flux. Alternate flux coating methods include screen printing, roll coating and tampo printing since only the tops of the bumps need to be coated.

FIG. 3 depicts a bumped wafer that has been provided with flux in the manner shown in FIGS. 2A and 2B. Specifically, FIG. 3 shows a wafer 12 having solder bumps 14 thereon. On each bump is a flux coating 16 which covers a portion of the bump. Once each bump 14 has been provided with a flux coating 16, the flux can be hardened by drying. As noted above, one preferred flux is a solid version of an epoxy/carboxylic acid type of flux commercially available as Chip Flux 20/20. The flux is dissolved in a solvent and provided with a wetting agent such as FC430, formerly available from Minnesota Mining and Manufacturing Co., or Fluowet, a low surface tension surfactant available from Hoechst-Celanese, to provide the deposited flux with a low surface energy.

After the solder bumps 14 have been provided with a flux coating 16, the spaces on the wafer surface between the solder bumps 14 are provided with an underfill in the liquid phase. The liquid underfill is applied to the wafer by spin coating, screen printing, or any of the common methods for applying liquids to surfaces. The resulting device is depicted in FIG. 4. Specifically, FIG. 4 shows a wafer 12 having solder bumps 14 each having a flux coating 16. The underfill material 18 is deposited on the wafer 12 in the spaces between the solder bumps 14. Since the flux coating 16 has a low surface energy, the underfill 18 does not become a coating over the flux 16. This is because surface chemistry principles require that wetting will only occur if the surface energy of the liquid (i.e., the underfill 18) is lower than that of the solid surface (i.e., the flux coating 16). Since the materials are selected such that the flux liquid has a higher surface energy than the flux coating, a receding contact angle results at the interface between the flux coating 16, the underfill 18, and the surrounding air. This is shown at region 15 of FIG. 4. Even though the underfill 18 may not wet the dried flux coating 16, the flux coating will still readily wet the bond pads on the circuit board to which the wafer is applied. This is a result of the effect that, when heat is applied, the flux coating 16 melts and becomes a liquid with a low surface energy. Again, since the flux liquid will have a lower surface energy than the bond pads, the flux liquid readily wets them. In addition, if desired, the flux coating 16 can be provided with various wetting additives such as the aforementioned FC430 or Fluowet. Alternatively a silicone such as Silwet L-77 available from Union Carbide could be employed.

In an alternative embodiment shown in FIG. 5, the flux coating 16 may be applied to the solder bumps 14 in a manner such that it entirely covers them. Upon heating for the purpose of soldering the chip to the circuit board, the flux will melt and readily wet the bond pads. The softened underfill, being a thermoplastic material, will flow in around the bump as the flux flows away. As such, any residual flux will not act as a contaminant having a tendency to reduce adhesion.

In another embodiment of the present invention, the underfill acts as a mask during application of the solder bumps. In this embodiment, a coatable underfill material, (typically a composite of a dissolved polymer and a solid filler in a solvent) is applied to the wafer surface prior to application of any solder bumps. It is important that the material selected for application has properties suitable for use as a flip chip underfill, or at the very least, can develop such properties during reflow solder assembly processing. The preferred material is a thermoplastic, such as Staystik™, commercially available from Alpha Metals, Inc. This material is then modified with a predetermined amount of an appropriate filler to provide the underfill with a

coefficient of thermal expansion (CTE) that approximates that of the solder joints which will be formed by the bumps. A mineral filler such as silicon dioxide is preferred. The preferred CTE of the resulting underfill material is approximately 25 ppm/°C, although values of up to about 45 ppm/°C are also envisioned. Even after processing the CTE of the underfill cannot become greater than about 60 ppm/°C, because this can cause detrimental thermomechanical stresses at the solder joints.

The preferred filler material is spherical and has a diameter less than the high of the solder bumps that will be applied to the wafer. Thus, as typical filler ranges in size from about 3 microns to about 15 microns. While silicon dioxide is preferred because of its ready availability, other non-electrically conductive materials such as aluminum nitride, aluminum oxide and beryllium oxide can be use as well.

A solvent, or solvent blend, which is compatible with each of the components is selected. Among the suitable solvents are included many common oxygenated, nitrogen-containing solvents as well as many polar aromatic solvents. The particular solvent system chosen should have evaporation and boiling points that allow removal of the solvent in the environment of a drying oven once the wafer is coated with the underfill material. Suitable solvents can be found in the Staystik pastes available from Alpha Metals, Inc.

In use, the underfill material is applied directly to the face, or active, side of the wafer prior to bumping. Semiconductor wafers typically have access, or bonding, pads formed of aluminum. Such pads are typically made solderable prior to bumping and, in this case, prior to applying the underfill material. The access pads are rendered solderable by depositing a solderable finish, often referred to as under bump metallization (UBM). Several UBM processes are commercially available, as are third-party UBM services provided by vendors. In the UBM process, the solderable finish is usually applied to the aluminum access pads using either vacuum deposition or chemical plating.

The underfill solution can be formulated to have the correct rheology for application to the wafer using any of a number of methods. For example, since the ratio of solvent to solids in the solution determines the viscosity of the solution, it is possible to formulate underfill solutions that can be applied using different methods. Since the solvent is substantially entirely evaporated after application of the underfill solution to the wafer, the resulting, solid underfill layer can have the composition regardless of the initial viscosity and percent solids of the underfill solution. This results because the solvent acts simply as a vehicle for carrying the solids during underfill application.

In one method, the underfill solution can be applied by spin coating, a common semiconductor processing method in which liquid is deposited onto a spinning wafer in order to provide a smooth and level coating. An underfill having a viscosity in the range of about 80-85 Kcps, measured at 2.5 RPM using an RVT #6 spindle on a Brookfield viscometer, has been found to give good results. When applied to a wafer, a wafer spin rate of about 1200 RPM yields a smooth coating.

A second method is stencil printing. This method requires a more viscous material that is produced using less solvent. The thixotropic index, (i.e., change in viscosity as a result of mechanical shearing), can also be adjusted, using thixotropic additives, to improve printing characteristics. The thickness of the stencil determines the amount of material applied to the wafer. Likewise, the amount of solvent contained in the underfill solution determines the amount of thickness reduction that occurs in the underfill during drying and solvent evacuation. Thus, it is necessary to consider both the stencil thickness and the solvent percent of the underfill solution in order to precisely control the thickness of the applied underfill. A dry underfill thickness range of about 25 to about 125 microns is suitable and will depend on the height of the bumps to be produced at a later stage. The thickness of the underfill layer is selected to preferably be from about 50 to about 80% of the bump height to allow form the bumps to collapse during the solder reflow step.

It should be understood that while spin coating and stencil printing are preferred, many other methods can be used to apply the underfill to the layer. These include, but are not limited to, needle deposition, spraying, screen printing and others.

The coating is then dried by heating it in an oven or by direct heating of the wafer. It has been found to be advantageous to heat the wafer while simultaneously using a forced hot air oven to help drive solvent out of the coating. Combined top and bottom heating can eliminate any tendency to trap solvent in the underfill layer by a process known as "skinning" in which the surface of the underfill material dries prematurely and forms a film (i.e., a skin) that acts as a barrier to further solvent evacuation. If drying is carried out properly, the resulting underfill material is non-tacky and amenable to handling.

Alternatively, the coating composition can be cast onto a release paper and then dried into a film. The film can be cut into a proper shape, called a preform, and applied to the wafer. Heating, with the application of pressure, will cause the underfill layer to bond to the wafer.

In order to apply the solder bumps to the underfill-coated wafer, openings must be formed in the underfill film at each interconnect pad location. In one preferred embodiment, the

openings are formed using laser machining techniques. Excimer lasers, for example, can be used to create openings in polymeric films by a photoablation process in which ultra-violet radiation causes the long-chain polymers to break down into small volatile by-products. Patterning can be achieved using either a pattern mask or a directed beam. Optical defraction grating patterning methods are also available. Photoablation is particularly suitable for the present application because it occurs with only a minimum amount of heating and does not damage the wafers. The process parameters can be set so that machining stops when the metal layer below the underfill is exposed, thereby making the process self-limiting. This is not always necessary, however, since many metals are resistant to laser ablation. Although UV lasers are preferred, other lasers, such as infrared (IR) lasers can be used as well.

Bumps of a suitable solder alloy are next applied to the wafer using the underfill as a mask which exposes only those section of the wafer which are to have solder bumps applied, i.e., the exposed pad areas of the wafer. Any bumping methods that do not require mask removal may be employed. In one embodiment, electroless plating can be used. Although the method does not typically require a mask, a high aspect ratio of plated material can be provided using the mask, and in the case of solder bumps, such high aspect ratios are desirable. In cases in which a zincate-electroless nickel process is employed, under bump metallization (described above) can be eliminated since the zincate treatment makes the aluminum platable by nickel.

Bumps made only from solder may be made by starting with solder pastes that are widely available. Stenciling, screen printing, pin transfer and other methods can also apply solder paste. Once the paste has been applied, the bump is formed by melting (i.e., reflowing) the paste. It is necessary to control the conditions at this point, however, because the underfill can soften or even liquefy into a viscous state if it is heated too much during the solder reflow process.

Other solder bumping methods include metal fluid jetting, or inverting the wafer and passing it over a solder wave or fountain of molten solder.

Flux is deposited onto the protruding solder bumps since it is not required on the face of the die. Since the solder bumps protrude above the surface of the underfill material, a number of methods can be used. For example, a thin layer of liquid flux can be coated onto a flat plat of glass. The wafer is then placed, bumps down, onto the thin film of flux and then withdrawn. A thin coating of flux, which can be subsequently dried, will remain on the bumps. Other methods such as roller coating, screen printing and tamp printing can be used as well.

At this stage, the wafer is ready to be diced, or singulated, to produce individual flip chips. Any of a wide variety of the methods known in the art for dicing wafers can be employed

to that end. The sole requirement of the inventive wafers is that the process be such that it does not interfere with the underfill material applied to the wafer/chip surfaces.

Once diced, individual flip chips may now be bonded to circuit boards and the like. The flip chip is placed and aligned to the bond pads of a substrate. As used herein, the term "substrate" is intended to mean a circuit board, a chip carrier, another semiconductor device or a metal lead frame. It is not necessary to add flux, although flux may be added for special reasons such as compensating for excessive oxide on substrate pads, or the need to hold the flip chip in place during assembly.

The positioned chip is then run through a solder reflow line commonly used for assembly. A multi-zone oven, with individual heat controls that permit a heating profile is preferred. The flux melts at a temperature ranging from about 80°C to about 140°C. The melting point is determined by selecting fluxes having epoxy resins with the appropriate melting point. Flux composition will be described in greater detail below. At higher temperatures, the underfill softens and may also melt depending upon the resin selected. Like the fluxes, underfill composition will be described in greater detail below. The solder bumps finally melt and form metallurgical joints to the substrate.

Alternatively, a standard flip chip bonder that can apply heat and pressure can be employed instead of the reflow oven. In that embodiment, the flip chip coated with the flux and underfill is placed into contact with the conductive pads on the circuit board and heat from the bonder head will activate the flux, form joints by reflowing the solder bumps, and cause the underfill and flux system to bond tightly to the board. The use of a standard flip chip bonder would allow a flip chip to be assembled to a board that already contained mounted components. This method could also be used to assemble a chip at a site that is being reworked.

The present invention recognizes that flux is required only at the areas of the solder bumps, and not in the spaces in between those connecting elements. Thus, the present invention separates the flux from the underfill in the regions between the solder bumps. Furthermore, by maintaining the flux and underfill as separate entities, additives tailored to each individual component may be added to provide both the flux and the underfill with desired properties. For example, the underfill can be a thermoplastic that de-bonds at elevated temperatures, or the flux layer can be designed to de-bond. As an alternative, the flux can convert to a strongly-bonded polymer after its mission as a flux has been accomplished, and the underfill can have the de-bonding properties. As such, a system in which the flux and underfill are maintained as separate entities is extremely versatile.

The invention can be further understood with reference to the attached Figures. As can be seen schematically in FIG. 6, a semiconductor device 110 comprises a portion of a semiconductor wafer 112 having an underfill material 114 applied to one surface thereof. The wafer 112 further includes a plurality of connection pads 115 which, ultimately, will contact the solder bumps and provide an electrical connection between the bumps and the underlying wafer circuitry. The underfill material has been applied to the surface upon which the solder bumps will be formed.

In FIG. 7, the underfill material 114 has been processes to form a plurality of apertures 116 through its depth. The apertures 116 are positioned precisely at the connection pads 115 on the wafer 112. Thus, as solder material fills the apertures, it will contact the connection pads 115 on the surface of the wafer. By providing the apertures 116 in the underfill material 114, the underfill material 114 is formed into a mask for applying the solder bumps. As such, the need for a separate mask to position the solder bumps is eliminated, because the underfill material serves the masking role as well as the underfilling role.

In FIG. 8, the solder bumps have been applied to the device 110. In particular, each of the apertures 116 in the underfill material 114 has been filled by a solder bump 118. The bumps 118 electrically contact the wafer 112 through the connection pads 115, and extend a slight distance above the underfill material 114 as well.

FIG. 9 shows the device 110 after the application of a flux material 120. As can be seen in the Figure, the flux 20 covers the entire exposed, bumped surface of the device 110. An alternative embodiment is shown in FIG. 10. In that Figure, the flux 120' does not cover the entire bumped surface of the device 110, but rather, covers only the portion of the bumps 118 that extends above the underfill material 114. As such, flux 120' will be present only in the precise areas in which it is needed, rather than over the entire exposed, bumped surface of the device 110.

The following Examples will help to illustrate the invention further.

Examples

Example 1: Flux

Flux Sample 1

Flux was made by blending the following with a high speed dispersing mixer:

50 wt% PMA solvent (1-methoxy-2-propyl acetate); from Dow

45 wt% EPON 1001F (Bisphenol A Epoxy); Shell

3 wt% Succinic Anhydride, Lonza

2 wt% Thixatrol ST (thickener); from Rheox

Flux Sample 2

Same mix as above but 0.1 to 0.5 wt% wetting agent (FC430 or Fluowet OTN) was added to reduce any tendency of the underfill to wet over the flux-coated bumps.

Flux Sample 3

45 grams PMA solvent 1-methoxy-2-propyl acetate); from Dow

48 grams EPON 1001F (Bisphenol A Epoxy); Shell

5 grams Adipic Acid, Aldrich Chemical

2 grams Thixatrol ST (thickener); from Rheox

The resulting fluxes had viscosities of about 750 kcps. Viscosity can easily be adjusted by varying the amount of the thixotropic agent. A useful range for fluxes to be used in applications of the present invention is about 250 kcps to about 1,000 kcps.

Flux was applied to the bumps in each case by coating out the flux onto a glass plate so that the flux thickness was 2 to 3 mils. The flip chips were dipped into the flux and removed with flux clinging to the bumps. The flux was dried by placing the chip upright in an oven at about 150° C for about 5 minutes. It is expected that this process will also work on a wafer.

Flux/Underfill sample 4

Staytik 383 paste (no filler) was dispensed onto the bumped side of the chip with a syringe and allowed to flow out before drying in a vacuum oven at about 70° C for about 30 minutes. The dry film thickness was less than the bump height. Bumps that were coated with flux containing the low surface tension wetting agent gave the best results with little or no underfill remaining on top of the bumps. Although soldering can still occur even with underfill on top of the bumps, the best results occur when only flux coats the upper bump surfaces.

Test Set 1

Flip chips, only coated with the three fluxes described above and no underfill, were used in the first set of tests intended to confirm good flux action. Each flux-coated chip was placed with bumps down onto a 1" diameter copper disk that was not pre-cleaned and therefore had a tarnished appearance. The samples were placed on a hot plate at about 216 °C for about 3 minutes. The flux and solder bumps melted causing the chip to attach to the copper. The copper became shiny in the areas contacted by the flux.

Samples were also run through an Electrovert Atmos 2000 convection oven with a peak temperature of approximately 220° C. It was found that the chips were soldered to the copper upon removal from the oven.

Test 2

Flip chips coated with both flux and underfill were run through the Electrovert oven at about 216° C peak temperature. Solder joints formed at the copper interface and the underfill also bonded.

Example 2: Thermoplastic Reworkable Underfill Coating Solution

100 grams of Staystik 908 (a 20% solids phenoxy solution) was blended with 30 grams of silica filler (FB-35 from Denka Ltd., Tokyo, Japan) using a high shear type mixer (Cowels Dissolver run at 2500 rpm) for 2 minutes. Entrapped air bubbles were allowed to dissipate prior to using the solution as a coating solution.

The resulting material was spin-coated onto an unbumped wafer mounted on a wafer coating machine (SCS Coater P6204-A). The coating was then dried using the following profile: 50° C for 20 minutes, 80° C for 30 minutes, 110° C for 30 minutes. The resulting fill was found to be smooth and dry.

Subsequently, openings were produced in the dry film layer using laser machining. Eutectic solder bumps were then formed in the openings. This was accomplished by applying solder paste to pad areas on the wafer using stencil printing, and then reflowing the solder to form the bumps. A flux was then applied to the bumps.

Example 3: Flux/Underfill Preparation

40% by weight bisphenol A epoxy resin (Shell, Epon 1007F) and 45% by weight dipropylene glycol methyl ether acetate, were blended together with 5% by weight hydrogenated castor oil. The blend was cooled to 25° C. Following the cooling step, 10% by weight adipic acid was dispersed in the blend using a high speed mixer.

The resulting flux is useful for coating onto solder bumps and the entire exposed, bumped surface of a wafer, including the underfill. Alternatively, the flux can be applied to the bumps only. Once applied, the flux is converted into a solid by drying it at about 60° C for 30 minutes.

Equivalents

From the foregoing detailed description of the specific embodiments of the invention, it should be apparent that a unique flip chip having an underfill which also acts as a mask for the bump application process has been described. Although particular embodiments have been disclosed herein in detail, this has been done by way of example for purposes of illustration only,

and is not intended to be limiting with respect to the scope of the appended claims which follow. In particular, it is contemplated by the inventor that various substitutions, alterations, and modifications may be made to the invention without departing from the spirit and scope of the invention as defined by the claims.

CLAIMS

1. An integrated circuit assembly which comprises:
   a) a substrate having a plurality of solderable contact sites on a surface thereof;
   b) a plurality of solder bumps positioned on the substrate such that each of the solderable contact sites has one solder bump associated therewith, the solder bumps being affixed to the solderable contact sites;
   c) a flux material which covers at least a portion of each solder bump; and
   d) an underfill material applied to the surface of the substrate, the underfill material occupying a space defined between each of the solder bumps and being of a depth such that at least a flux covered portion of each solder bump extends therethrough.

2. The integrated circuit assembly of claim 1 wherein the substrate comprises a semiconductor wafer.

3. The integrated circuit assembly of claim 2 wherein the substrate comprises a semiconductor chip.

4. The integrated circuit assembly of claim 3 wherein the substrate comprises a flip chip.

5. The integrated circuit assembly of claim 1 wherein the flux covers substantially all of each solder bump.

6. The integrated circuit assembly of claim 1 wherein the flux comprises an epoxy resin and a material selected from the group consisting of carboxylic acids, anhydrides and combinations thereof.

7. The integrated circuit assembly of claim 1 wherein the underfill material is reworkable.

8. The integrated circuit assembly of claim 7 wherein the underfill material comprises a thermoplastic material.

9. The integrated circuit assembly of claim 8 wherein the thermoplastic material is selected from the group consisting of phenoxy resins, acrylic resins, methacrylic resins,

polycarbonate resins, polyamide resins, polybutene resins, polyester resins, polyolefin resins and mixtures thereof.

10. A method for making an integrated circuit assembly which comprises:

a) providing a substrate having a plurality of solderable contact sites on a surface thereof;

b) positioning a plurality of solder bumps on the substrate such that each of the solderable contact sites has one solder bump associated therewith;

c) affixing each solder bump to its associated contact site;

d) applying a flux material to the solder bumps in a manner such that at least a portion of each solder bump is provided with flux; and

e) applying an underfill material to the surface of the substrate in a manner such that it occupies a space defined between each of the solder bumps and is of a depth such that at least a flux covered portion of each solder bump extends therethrough.

11. The method for making an integrated circuit assembly of claim 10 wherein the substrate comprises a semiconductor wafer.

12. The method for making an integrated circuit assembly of claim 11 wherein the substrate comprises a semiconductor chip.

13. The method for making an integrated circuit assembly of claim 12 wherein the substrate comprises a flip chip.

14. The method for making an integrated circuit assembly of claim 10 wherein the flux covers substantially all of each solder bump.

15. The method for making an integrated circuit assembly of claim 10 wherein the flux comprises an epoxy resin and a material selected from the group consisting of carboxylic acids, anhydrides and combinations thereof.

16. The method for making an integrated circuit assembly of claim 10 wherein the underfill material is reworkable.

17. The method for making an integrated circuit assembly of claim 16 wherein the underfill material comprises a thermoplastic material.

18. The method for making an integrated circuit assembly of claim 17 wherein the thermoplastic material is selected from the group consisting of phenoxy resins, acrylic resins, methacrylic resins, polycarbonate resins, polyamide resins, polybutene resins, polyester resins, polyolefin resins and mixtures thereof.

19. A method for affixing a flip chip to a circuit board which comprises the steps of:
    a) providing a printed circuit board having a plurality of solderable contact sites on a surface thereof;
    b) providing an integrated circuit chip having a plurality of solderable contact sites on a surface thereof, each solderable contact site on the integrated circuit chip having a corresponding solderable contact site on the surface of the printed circuit board, the integrated circuit chip further characterized in that it includes:
        i) a plurality of solder bumps positioned on the integrated circuit chip such that each of the solderable contact sites located on the surface of the integrated circuit chip has one solder bump associated therewith, the solder bumps being affixed to the solderable contact sites;
        ii) a flux material which covers at least a portion of each solder bump; and
        iii) an underfill material applied to the surface of the substrate, the underfill material occupying a space defined between each of the solder bumps and being of a depth such that at least a flux covered portion of each solder bump extends therethrough;
    c) positioning the integrated circuit chip relative to the printed circuit board such that each solder bump is in contact with a solderable contact site on the printed circuit board;
    d) heating the integrated circuit chip to a temperature sufficiently high to melt the solder and the underfill material; and
    e) allowing the solder and underfill material to solidify.

20. An integrated circuit assembly which comprises:
    a) a substrate having a plurality of solderable contact sites on a surface thereof;

b) a plurality of solder bumps positioned on the substrate such that each of the solderable contact sites has one solder bump associated therewith, the solder bumps being affixed to the solderable contact sites; and

c) an underfill material applied to the surface of the substrate, the underfill material occupying a space defined between each of the solder bumps and being of a depth such that at least a portion of each solder bump extends therethrough.

21. An integrated circuit assembly which comprises:

a) a substrate having at least one solderable contact site on a surface thereof; and

b) an underfill material applied to the surface of the substrate, the underfill material substantially entirely covering the surface of the substrate having the solderable contact site.

22. An integrated circuit assembly which comprises:

a) a substrate having at least one solderable contact site on a surface thereof; and

b) an underfill material applied to the surface of the substrate, the underfill material substantially entirely covering the surface of the substrate having the solderable contact site except at the solderable contact site itself, thereby allowing the underfill to act as a mask exposing substantially only the solderable contact site on the substrate surface.

23. A method of making an integrated circuit assembly which comprises the steps of:

a) providing a substrate having at least one solderable contact site on a surface thereof;

b) applying an underfill material to the substrate surface in a manner which substantially entirely covers the substrate surface and the solderable contact site;

c) treating the underfill material to form at least one aperture therein, the at least one aperture extending substantially entirely through the underfill material and being located such that it exposes only the solderable contact site;

d) applying at least one solder bump to the assembly in a manner such that a bump occupies each aperture in the underfill, contacts the exposed solderable contact site therein, and extends above the underfill material; and

e) applying a flux to the surface, the flux covering at least the exposed portions of the solder bumps.

24. The method of claim 23 wherein the substrate comprises a semiconductor wafer.

25. The method of claim 24 wherein the substrate comprises a semiconductor chip.

26. The method of claim 25 wherein the substrate comprises a flip chip.

27. The method of claim 23 wherein the flux covers substantially the entire surface upon which the solder bumps are exposed.

28. The method of claim 23 wherein the flux comprises an epoxy resin and a material selected from the group consisting of carboxylic acids, anhydrides and combinations thereof.

29. The method of claim 23 wherein the underfill material is reworkable.

30. The method of claim 29 wherein the underfill material comprises a thermoplastic material.

31. The method of claim 30 wherein the thermoplastic material is selected from the group consisting of phenoxy resins, acrylic resins, methacrylic resins, polycarbonate resins, polyamide resins, polybutene resins, polyester resins, polyolefin resins and mixtures thereof.

32. The method of claim 23 wherein the apertures are formed using photoablation.

33. The method of claim 32 wherein the apertures are formed using a laser.

34. The method of claim 33 wherein the laser is selected from the group consisting of excimer lasers, UV lasers and infrared lasers.

35. The method of claim 33 wherein the apertures are formed using a directed laser beam.

36. The method of claim 33 wherein the apertures are formed using a pattern mask.

37. A method for affixing an integrated circuit chip to a substrate which comprises the steps of:

a) providing a substrate having a plurality of solderable contact sites on a surface thereof;

b) providing an integrated circuit chip having a plurality of solderable contact sites on a surface thereof, each solderable contact site on the integrated circuit chip having a corresponding solderable contact site on the surface of the printed circuit board, the integrated circuit chip further characterized in that it was made by a process including the steps of:

i) providing a semiconductor wafer having at least one solderable contact site on a surface thereof;

ii) applying an underfill material to the wafer surface in a manner which substantially entirely covers the wafer surface and the solderable contact site;

iii) treating the underfill material to form at least one aperture therein, the at least one aperture extending substantially entirely through the underfill material and being located such that it exposes only the solderable contact site on the wafer;

iv) applying at least one solder bump to the assembly in a manner such that a bump occupies each aperture in the underfill, contacts the exposed solderable contact site therein, and extends above the underfill material;

v) applying a flux to the surface, the flux covering at least the exposed portions of the solder bumps; and

vi) dividing the wafer into at least one integrated circuit chip;

c) positioning the integrated circuit chip relative to the printed circuit board such that each solder bump is in contact with a solderable contact site on the printed circuit board;

d) heating the integrated circuit chip to a temperature sufficiently high to melt the solder and the underfill material; and

e) allowing the solder and underfill material to solidify.

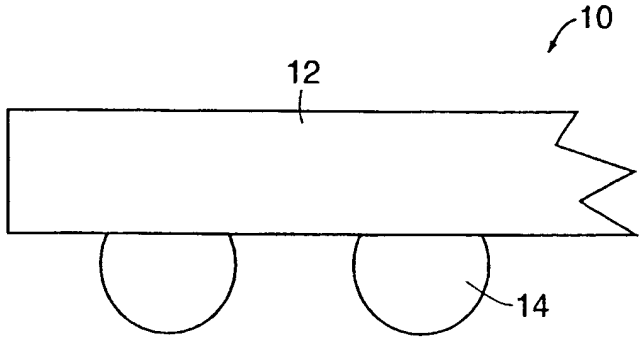

FIG. 1

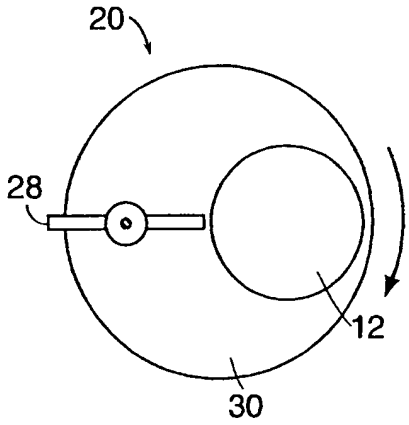

FIG. 2A

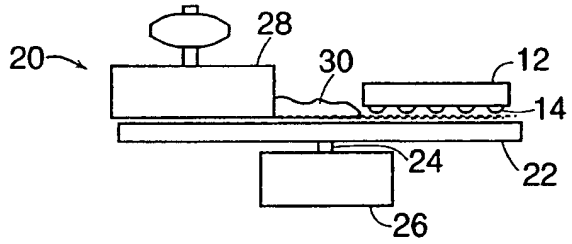

FIG. 2B

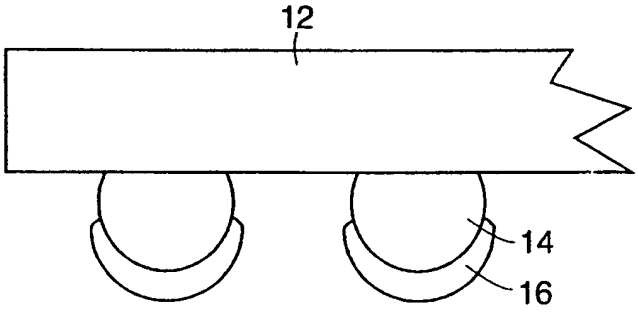

FIG. 3

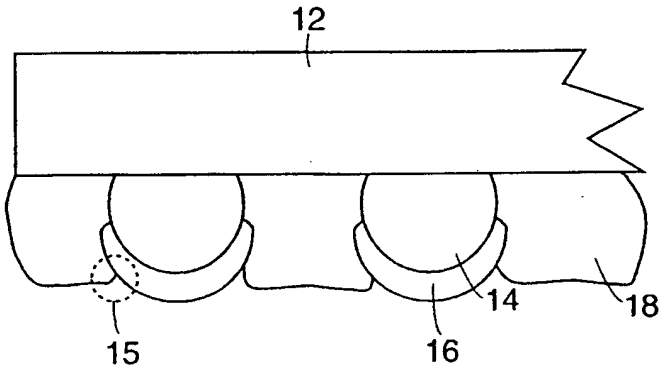

FIG. 4

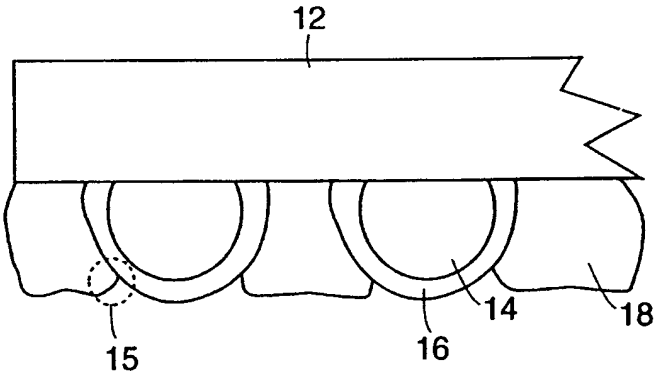

FIG. 5

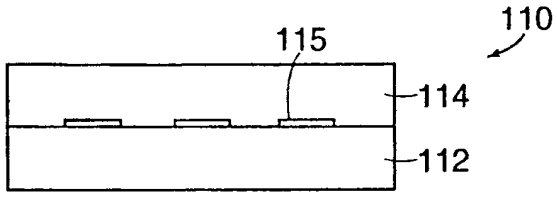

FIG. 6

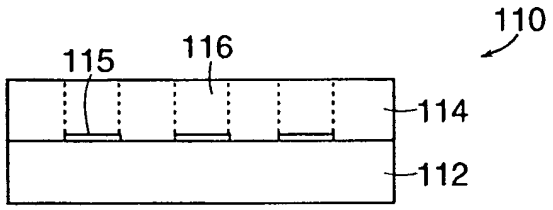

FIG. 7

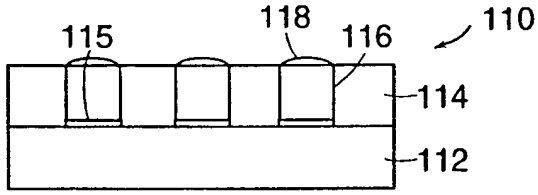

FIG. 8

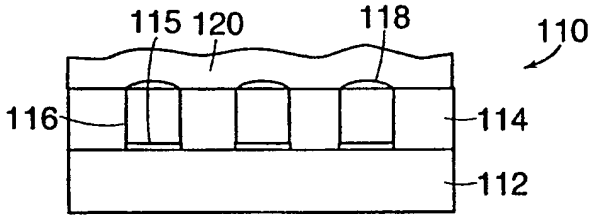

FIG. 9

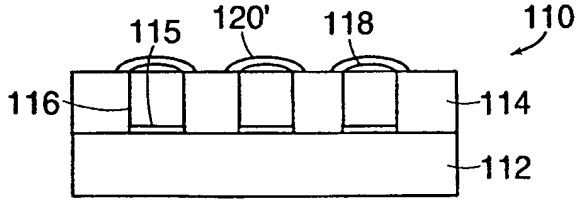

FIG. 10

INTERNATIONAL SEARCH REPORT

ernational Application No
PCT/US 99/08812

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/56 H01L21/60

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X	EP 0 853 337 A (FUJITSU LTD) 15 July 1998 (1998-07-15) column 2, line 12 - line 13 column 5, line 31 - line 41 column 36, line 11 - column 42, line 46 figures 1-9	20,21
P,A		1-4, 10-13, 32-36
X	& WO 98 02919 A (FUJITSU LTD) 22 January 1998 (1998-01-22)	20,21
A		1-4, 10-13, 32-36

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
- 12 August 1999	19/08/1999

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